IN THE CLAIMS

Please status of the claims is as follows.

1. (Currently Amended) A system for reducing power consumption in digital circuits using charge redistribution, comprising:

a plurality of signal lines;

an intermediate floating virtual source/sink, and

a charge redistribution circuit connected to a source and a load portion of at least one of said signal lines that isolates the load portion of said line from its source by entering a high impedance state and that connects it to the intermediate floating virtual source/sink during an idle period prior to a change of state,

wherein the charge redistribution circuit comprises a transition detector connected to the source of one of the signal lines and having two outputs, a first of the outputs connected to an input of a tri-state driver circuit, a second of the outputs for simultaneously (i) enabling the tri-state driver circuit to enter the high impedance state and (ii) enabling a control switch to connect an output of the tri-state driver circuit to the floating virtual source/sink whenever a transition is detected on the signal line, the output of the tri-state driver circuit coupled to the load portion of the signal line, and

wherein the transition detector comprises a delay circuit having its input connected to the source of the signal line and its output connected to the first output of the transition detector and to a first input of a 2-input exclusive-OR or exclusive-NOR gate while a second input of the gate is directly connected to the source of the signal line and its output is connected to the second output of the transition detector.

2. (Original) The system as claimed in claim 1 wherein the intermediate floating virtual source/sink comprises a charge storage element.

3. (Currently Amended) The system as claimed in claim 1 wherein the intermediate floating virtual source/sink is initially discharged ~~the charge redistribution circuit comprises a transition detector connected to the source of one of the signal lines and having two outputs, a first of the outputs connected to an input of a tri-state driver circuit, a second of the outputs for simultaneously (i) enabling the tri-state driver circuit to enter the high impedance state and (ii) enabling a control switch to connect an output of the tri-state driver circuit to the floating virtual source/sink whenever a transition is detected on the signal line, the output of the tri-state driver circuit coupled to the load portion of the signal line~~.

4. (Previously Presented) The system as claimed in claim 2 wherein the charge storage element comprises a capacitor or a set of capacitors.

5. (Currently Amended) The system as claimed in claim 1 wherein the intermediate floating virtual source/sink is charged during the change of state ~~3 wherein the transition detector comprises a delay circuit having its input connected to the source of the signal line and its output connected to the first output of the transition detector and to a first input of a 2-input exclusive-OR or exclusive-NOR gate while a second input of the gate is directly connected to the source of the signal line and its output is connected to the second output of the transition detector~~.

6. (Previously Presented) The system as claimed in claim 4 wherein the capacitor comprises a floating conductor or a floating conducting mesh optionally coupled to capacitor elements.

7. (Currently Amended) An integrated circuit for reducing power consumption in digital circuits using charge redistribution, comprising:

a plurality of signal lines;

an intermediate floating virtual source/sink, and

a charge redistribution circuit connected to a source and a load portion of at least one of said signal lines that isolates the load portion of said line from its source by entering a high impedance state and that connects it to the intermediate floating virtual source/sink during an idle period prior to a change of state,

wherein the charge redistribution circuit comprises a transition detector connected to the source of one of the signal lines and having two outputs, a first of the outputs connected to an input of a tri-state driver circuit, a second of the outputs for simultaneously (i) enabling the tri-state driver circuit to enter the high impedance state and (ii) enabling a control switch to connect an output of the tri-state driver circuit to the floating virtual source/sink whenever a transition is detected on the signal line, the output of the tri-state driver circuit coupled to the load portion of the signal line, and

wherein the transition detector comprises a delay circuit having its input connected to the source of the signal line and its output connected to the first output of the transition detector and to a first input of a 2-input exclusive-OR or exclusive-NOR gate while a second input of the gate

is directly connected to the source of the signal line and its output is connected to the second output of the transition detector.

8. (Original) An integrated circuit as claimed in claim 7 wherein the intermediate floating virtual source/sink comprises a charge storage element.

9. (Currently Amended) An integrated circuit as claimed in claim 7 wherein the intermediate floating virtual source/sink is initially discharged ~~the charge redistribution circuit comprises a transition detector connected to the source of one of the signal lines and having two outputs, a first of the outputs connected to an input of a tri-state driver circuit, a second of the outputs for simultaneously (i) enabling the tri-state driver circuit to enter the high impedance state and (ii) enabling a control switch to connect an output of the tri-state driver circuit to the floating virtual source/sink whenever a transition is detected on the signal line, the output of the tri-state driver circuit coupled to the load portion of the signal line~~.

10. (Previously Presented) An integrated circuit as claimed in claim 8 wherein the charge storage element comprises a capacitor or a set of capacitors.

11. (Currently Amended) An integrated circuit as claimed in claim 8 wherein the intermediate floating virtual source/sink is charged during the change of state ~~9 wherein the transition detector comprises a delay circuit having its input connected to the source of the signal line and its output connected to the first output of the transition detector and to a first input of a 2-input exclusive-OR or exclusive-NOR gate while a second input of the gate is directly~~

~~connected to the source of the signal line and its output is connected to the second output of the transition detector~~.

12. (Original) An integrated circuit as claimed in claim 10 wherein the capacitor comprises a floating conductor or a floating conducting mesh optionally coupled to capacitor elements.

13. (Currently Amended) A method for reducing power consumption in digital circuits using charge redistribution, comprising the steps of:

providing a plurality of signal lines;

providing an intermediate floating virtual source/sink, and

isolating a load portion of at least one of said signal lines from its source by (i) placing a charge redistribution circuit connected to the source and the load portion of one of the signal lines in a high impedance state and (ii) connecting the load portion of the signal line to the intermediate floating virtual source/sink during an idle period prior to a change of state,

wherein the charge redistribution circuit comprises a transition detector connected to the source of one of the signal lines and having two outputs, a first of the outputs connected to an input of a tri-state driver circuit, a second of the outputs for simultaneously (i) enabling the tri-state driver circuit to enter the high impedance state and (ii) enabling a control switch to connect an output of the tri-state driver circuit to the floating virtual source/sink whenever a transition is detected on the signal line, the output of the tri-state driver circuit coupled to the load portion of the signal line, and

wherein the transition detector comprises a delay circuit having its input connected to the source of the signal line and its output connected to the first output of the transition detector and to a first input of a 2-input exclusive-OR or exclusive-NOR gate while a second input of the gate is directly connected to the source of the signal line and its output is connected to the second output of the transition detector.

14. (Previously Presented) The method as claimed in claim 13 wherein the step of providing an intermediate floating virtual source/sink comprises supplying a charge storage element.

15. (Original) The method as claimed in claim 13 wherein the change of state is identified by detecting a transition on the signal line.

16. (Original) The method as claimed in claim 14 wherein the charge storage element is supplied by connecting a capacitor or a set of capacitors.

17. (Previously Presented) The method as claimed in claim 15 wherein the transition is detected by exclusive-NORing or exclusive-ORing a signal on the signal line with a delayed version of the signal.

18. (Previously Presented) The method as claimed in claim 15 wherein the load portion of the signal line is connected to the intermediate floating virtual source/sink whenever the transition is detected.

19. (Original) The method as claimed in claim 16 wherein the capacitor is provided by a floating conductor or a floating conducting mesh optionally coupled to capacitor elements.

20. (Previously Presented) The method as claimed in claim 13, wherein isolating the load portion of the signal line from its source and connecting the load portion of the signal line to the intermediate floating virtual source/sink comprise:

placing a tri-state driver circuit in the charge redistribution circuit in the high impedance state; and

simultaneously enabling a control switch to connect an output of the tri-state driver circuit to the floating virtual source/sink, the output of the tri-state driver circuit coupled to the load portion of the signal line.